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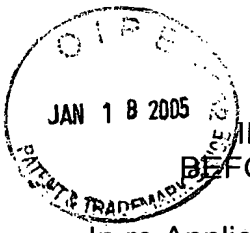

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Confirmation No. 7705
Andrew M. Jones	Art Unit: 2665
Serial No.: 09/410,974	Examiner: J. Philpott
Filed: October 1, 1999	Customer No. 30429
For: INTEGRATED CIRCUIT IMPLEMENTING PACKET TRANSMISSION (as amended)	Docket No. 99-TK-553SS

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Mail Stop Appeal Brief - Patents
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APPELLANT'S BRIEF UNDER 37 CFR 1.192

I. Real Party in Interest

STMicroelectronics, Inc.
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Carrolton, TX, 750003
USA

II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1, 3-10 and 12-20 are pending in the application. No claims have been allowed.

Claims 1, 3, 4, 6, 7, 9, 10, 12-14, 16, 17, and 19 were rejected under 35 U.S.C. 103 based upon Carson et al. in view of Katzman et al.

Claims 5, 8, 15, 18 and 20 were rejected under 35 U.S.C. 103 based upon Carson et al. in view of Katzman et al and further in view of Circello.

IV. Status of Amendments

All the claim amendments have been entered. Claims 1, 3-10 and 12-20 as pending are provided in the Appendix of Claims on Appeal.

V. Summary of the Invention

All references to the specification and drawings made in this section are with respect to the Substitute Specification filed on May 7, 2003.

As noted at paragraph [0003] of Appellant's Background, the invention addresses the need for a packet protocol that can be used across a number of different projects and designs, and that has compact encoding. In paragraph [0004] the specification teaches that the invention an integrated circuit (e.g., integrated circuit or chip 11 in Fig. 1 having of functional modules (e.g., M1, M2, M3 and M4 in Fig. 1A and Fig. 1B and described in paragraph [0022]) interconnected via a packet router (e.g., element 15 in Fig. 1A and 1B, shown in greater detail in Fig. 2).

A significant feature of the claimed invention is the implementation of routed, packet communications within an integrated circuit between functional modules on that integrated circuit. As noted in paragraph [0023], the routing bus is arranged to transmit request and response packets to the modules for effecting memory access transactions. Each functional module having packet handling circuitry (e.g., packet handling circuitry 2 shown in Fig. 2) for generating and receiving packets conveyed by the packet router (see, e.g., the description of packet handler 2 at paragraph

[0028]). A first set of functional modules, acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry (e.g., logic 200 in Fig. 2 and described at paragraph [0028]) for generating request packets for implementing transactions. Each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a packet type bit denotes the type of the packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function. A second set of the functional modules act as target modules that have packet handling circuitry which includes packet receiver logic (e.g., logic 206 in Fig. 2 and described at paragraph [0028]) for receiving the request packets and for generating respective response packets.

VI. Issues

1. Whether claims 1, 6 and 7 as well as claims 3, 4 and 17 that depend from them are made obvious by Carson et al. in view of Katzman et al. as required under 35 U.S.C. §103.

2. Whether claim 9 as well as claim 10 that depend from claim 9 are made obvious by Carson et al. in view of Katzman et al. as required under 35 U.S.C. §103.

3. Whether claim 12 as well as claims 13-14, 16 and 19 that depend from claim 12 are made obvious by Carson et al. in view of Katzman et al. as required under 35 U.S.C. §103.

4. Whether claims 5, 8, 15, 18 and 20 are made obvious by Carson et al. in view of Katzman et al. in combination with Circello under 35 U.S.C. §103(a).

VII. Grouping of Claims

The following groups of claims have been rejected by the Examiner.

Rejection under 103 based upon Carson et al. in view of Katzman et al:

Group I: claims 1, 3, 4, 6, 7 and 17 stand or fall together.

Group II: claims 9 and 10 stand or fall together.

GroupIII claims 12-14, 16 and 19 stand or fall together.

Rejection under 103 based upon Carson et al. in view of Katzman et al. and further in view of Circello:

Group IV: claims 5, 8, 15, 18 and 20 stand or fall together.

VIII. Argument

A. Rejection of claims 1, 3, 4, 6, 7 and 17 based upon Carson et al. in view of Katzman et al. as required under 35 U.S.C. §103 is Improper.

Independent claims 1, 6 and 7 call for, among other things, a plurality of functional modules formed within an integrated circuit that are interconnected via a packet router that is also formed within the integrated circuit. At least these features of independent claims 1, 6 and 7 are not shown or suggested by the relied on references.

During prosecution of this case the Examiner has alleges that Carson et al. and Katzman et al. show systems that involve multiple, separate integrated circuits and use packet communication to exchange messages between the separate integrated circuits. However, the Carson et al. reference does not show any "packets" nor does the word "packet" appear in the reference. Instead, Carson et al. show a plurality of IRQ lines (elements 16 in Fig. 1) that appear to carry an interrupt signal, but not a packet. Further, the packet constructions allegedly shown in Fig. 4 and Fig. 7 of Carson et al. are, as specified in the reference, data structures. Specifically, Fig. 4 shows a redirection table and Fig. 7 shows a command register. Neither of these data structures fairly shows or suggests a packet as is alleged in the rejections.

Moreover, the Examiner makes a citation to an Intel 82C59A and 82380 chip sets for support that the claimed features of claims 1, 6 and 7 are formed within an integrated circuit. While it is true that each of these devices is an integrated circuit, the description appearing in Carson et al. supports that these devices receive external interrupt requests, which must come from other, separate integrated circuits. This citation to Carson et al. and the Intel 82C59A and 82380 chips does not support the statement that the Examiner is trying to make. Nothing about the internal workings of

the Intel 82C59A and 82380 chips (set out in some detail in the material bridging columns 1 and 2 in Carson et al.) shows or suggests that either device includes a plurality of functional modules formed within an integrated circuit that are interconnected via a packet router that is also formed within the integrated circuit. Fig. 1 in Carson seems to militate against this suggestion in the Office Action in that it does not show or suggest modules that are interconnected by a packet router, nor does Fig. 1 show even a packet router, or packet handling circuitry.

The Examiner asserts that "Carson anticipates that the invention may be exemplified by an integrated circuit" because Carson is an improvement on the Intel 82C59A and/or 82480 chips. This assertion, however, is not supported in the references themselves. Moreover, the Intel 82C59A and/or 82480 were marketed as members of "chip sets", not stand-alone integrated circuits. Also, nothing in the Carson or Katzman or any other cited references suggests that the Intel 82C59A and/or 82480 used packet communication between functional modules of the Intel 82C59A and/or 82480 integrated circuits. Hence, Carson and Katzman taken alone or in combination suggest, at most, the conventional use of packet communication between separate integrated circuits.

The Examiner has cite In re Japiske, 86 USPQ 70 (CCPA 1950) as authority for a proposition that "it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a shown of unexpected results". However, this case has been clarified somewhat in the subsequent 55 years by analysis provided in the manual of patent examining procedure. The instruction of MPEP 2144.04 (VI)(C), entitled "Rearrangement of Parts," it is noted that "the mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims...is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason...to make the necessary changes..." In the instant case the Examiner fails to state any motivation for making the suggested change.

More fundamentally, the Office Action fails to even state what parts of the reference would be rearranged to meet the limitations of claims 1, 6 and 7. Is one supposed to rearrange the processors in Fig. 2 and place them inside the MPIC

controller 100 along with MPIC Bus 103? If so, where is there any suggestion to make such a change? What is the motivation to make such a change? Where is there any indication of an expectation of success in making such a change? It is respectfully believed that the Examiner has failed to state even a prima facie case of obviousness.

It is believed that it would take much more than mere rearrangement to transform the teachings of Carson and Katzman so as to meet the limitations of claims 1, 6 and 7. It is more appropriate to consider the instruction found at MPEP 2144.04 (V)(B) entitled "Making Integral". Here the MPEP sets out that integrating components into an integral mechanism is not, *per se*, obvious. *See, Schenck v. Nortron Corp.*, 218 USPQ 698 (Fed. Cir. 1983).

Based on the above remarks, Appellant respectfully requests that the rejection of claims 1, 3, 4, 6, 7 and 17 be reversed.

B. Rejection of claim 9 as well as claim 10 that depend from claim 9 based upon Carson et al. in view of Katzman et al. under 35 U.S.C. §103 is Improper.

Independent claim 9 calls for, among other things, an initiator functional module wherein both the initiator functional module and the packet router are formed within the integrated circuit. Similarly, independent claim 10 calls for a target functional module wherein both the target functional module and the packet router are formed within the integrated circuit. These features of claims 9 and 10 are not shown or suggested in the relied on combination of references. As noted above, Carson et al. in view of Katzman et al. relate exclusively to multi-chip computer systems and do not show or suggest a packet communication system within an integrated circuit. Only applicant teaches and claims the integration of these features in the particular manner set out in claims 9 and 10. For at least these reasons claims 9 and 10 are not anticipated or made obvious by the relied on references.

Claim 9 further calls for request packets to include an operation field denoting the function to be implemented by the request packet. The operation field comprises eight bits of which a single packet type bit denotes a request or response packet, four

operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function. As noted by the Examiner, these very specific limitations in claim 9 are not shown or suggested by the combined references. Claim 9 is nevertheless rejected by declaring these specific features of the operation family bits to be nothing more than numerical parameters or values whose modification would be obvious lacking criticality in a particular recited value. However, a significant goal of the invention of claim 9 is to provide a packet protocol that can be used across a number of different projects and designs, and that has compact encoding nevertheless provides rapid decoding of important information about the packet. As noted above with respect to the group I rejection, Carson et al do not show a packet having an associated destination ID and operation field because Carson et al. do not show any packets at all.

Moreover, even if the changes required to modify the 64-bit data structures of Carson et al. were within the ordinary skill in the art, there is no motivation to make such a change. The Examiner does not state any motivation to make such a change. Only Applicant provides motivation to use the compact yet efficiently decoded scheme called for in claim 9.

Claim 10, like claim 9, calls for a specific packet structure with specific bit assignments. These specific features of claim 10 are neither mere numeric parameters or values, nor is there any motivation supplied in the references or stated by the Examiner to modify the references in a manner that would meet the limitations of claim 10.

Based on the above remarks, Appellant requests that the rejection of claims 9 and 10 be reversed.

C. Rejection of claim 12 as well as claims 13-14, 16 and 19 that depend from claim 12 based upon Carson et al. in view of Katzman et al. under 35 U.S.C. §103 is Improper.

Independent claim 12 calls for, among other things, a method of implementing transactions between an initiator module within the integrated circuit, and generating a request packet within said integrated circuit. Carson et al. and Katzman et al. do not

show or suggest a method of implementing transactions within an integrated circuit, only transactions external to the integrated circuits and conducted between separate integrated circuits. For at least these reasons claim 12 is not anticipated or made obvious by the relied on references. Claims 13-14, 16 and 19 that depend from claim 12 are believed to be allowable for at least the same reasons as claim 12.

Further, claim 12 calls for an operation field having eight bits of which a single packet type bit denotes the type of a packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function. Claim 12, like claims 9 and 10 discussed in the Group II rejection, calls for a specific packet structure with specific bit assignments. These specific features of claim 12 provide a compact yet flexible and rapidly decoded protocol that is not merely an "adjustment" to the prior art. There is not any motivation supplied in the references or stated by the Examiner to modify the references in a manner that would meet the limitations of claim 12.

Based on the above remarks, Appellant requests that the rejection of claims 12-14, 16 and 19 be reversed.

D. Rejection of claims 5, 8, 15, 18 and 20 are made obvious by Carson et al. in view of Katzman et al. in combination with Circello under 35 U.S.C. §103 is Improper

Claims 5, 8, 15, 18 and 20 were rejected under 35 U.S.C. 103 based upon Carson et al. in view of Katzman et al and further in view of Circello. This rejection is respectfully traversed. Claims 5 and 18, which depend from claim 1, claim 8, which depends from claim 7 as well as claims 15 and 20 which depend from 12 are distinct from the combination of Carson and Katzman for at least the same reasons as claims 1, 7 and 12. Circello does not supply the deficiencies of Carson et al. and Katzman.

Specifically, Circello does not show or suggest functional modules within an integrated circuit that are coupled by a packet router, nor functional modules within an IC that have packet handling circuitry for communicating with other functional modules within the same IC, nor the implementation of target and initiator functional

modules. For at least these reasons, claims 5, 8, 15, 18 and 20 are neither anticipated nor made obvious by Carson et al., Katzman et al. and Circello either alone or in combination.

Based on the above remarks, Appellant requests that the rejection of claims 5, 8, 15, 18 and 20 be reversed.

Conclusion

In view of all of the above, claims 1-3, 8, and 21-24 are believed to be allowable and the case in condition for allowance. Appellant respectfully requests that the Examiner's rejections based on 35 U.S.C. 103 be reversed for all pending claims.

Respectfully submitted,

Date: January 18, 2005

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IX. APPENDIX OF CLAIMS ON APPEAL

1. An integrated circuit comprising:

a plurality of functional modules formed within said integrated circuit interconnected via a packet router formed within said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein at least a first set of said functional modules, acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of the packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function, and

wherein a second set of the functional modules, acting as target modules, each have packet handling circuitry which includes packet receiver logic for receiving said request packets and for generating respective response packets, wherein the single packet type bit distinguishes between request packets and response packets.

2. (Cancelled).

3. An integrated circuit according to claim 1, wherein the function in each request packet is a memory access operation.

4. An integrated circuit according to claim 3, wherein one of said operation family bits distinguishes between primitive memory access operations involving a single request packet and compound memory access operations involving a plurality of request packets.

5. An integrated circuit according to claim 1, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier.

6. An integrated circuit comprising:

a plurality of functional modules formed in said integrated circuit and interconnected via a packet router formed in said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein at least a first set of said functional modules acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of the packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function, and

wherein a second set of said functional modules, acting as target modules, each having packet handling circuitry which includes packet receiver logic for receiving said request packets and for generating respective response packets, wherein the single packet type bit distinguishes request packets and response packets.

7. An integrated circuit comprising:

a plurality of functional modules formed in said integrated circuit and interconnected via a packet router formed in said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein each functional module has packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, and packet receiver logic for receiving request packets and for generating respective response packets, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the packet, wherein the operation field comprises eight bits of which a single packet type bit distinguishes between request packets and

response packets, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function.

8. An integrated circuit according to claim 7, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier.

9. An initiator functional module for connection in an integrated circuit comprising:

an interface for supplying and receiving packets to and from the functional module, said interface being connected to a port for connecting the functional module to a packet router, wherein both the initiator functional module and the packet router are formed within the integrated circuit;

packet handling circuitry for handling said packets and including request packet generating logic which generates request packets for supply to the packet router via the interface, each request packet having a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes a request or response packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function.

10. A target functional module for connection in an integrated circuit comprising:

an interface for supplying and receiving packets to and from the functional module, said interface being connected to a port for connecting a functional module to a packet router, wherein both the target functional module and the packet router are formed within the integrated circuit;

packet receiver logic which is operable to receive request packets supplied from the packet router via the interface to the target functional module, each request packet having an operation field denoting the function to be implemented by the request packet, said operation field including four operation family bits denoting the function to be implemented by the packet, one of said operation family bits

distinguishing between primitive memory access operations and complex memory access operations, wherein the packet receiver logic comprises means for detecting the status of said one operation family bit to determine whether the memory access operation is primitive or compound; and

means for generating respective response packets on receipt of each request packet, wherein the operation field of both request and response packets includes a single packet type bit which distinguishes between request packets and response packets.

11. (Cancelled)

12. A method of implementing transactions in an integrated circuit comprising a plurality of functional modules interconnected via a packet router, the method comprising:

at one of said functional modules acting as an initiator module within said integrated circuit, generating a request packet including a destination indicator identifying a destination of the packet within said integrated circuit and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of a packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function;

at the destination indicated by the destination indicator, receiving said request packet and identifying the function to be implemented from the four operation family bits and the operation qualifier bits; and

generating a response packet for transmission to the initiator functional module, wherein the single packet type bit distinguishes between request packets and response packets.

13. A method according to claim 12, wherein the function in each request packet is a memory access operation.

14. A method according to claim 13, wherein one of said operation family bits distinguishes between primitive memory access operations involving a single request

packet and compound memory access operations involving a plurality of request packets, and wherein the method comprises detecting at the destination of the packet the status of this bit to determine whether a primitive memory access operation or a compound memory access operation is to be implemented.

15. A method according to claim 12, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier, the method comprising at the destination of the packet, detecting the size of said data object from the three bit operation qualifier to determine how to implement the function in the request packet.

16. A method according to claim 13, wherein said memory access operations include load, store, read-modify-write and swap operations.

17. An integrated circuit according to claim 3, wherein the memory access operation includes cache operations.

18. An integrated circuit according to claim 1, wherein the four operation family bits denote that the operation field is user defined.

19. A method according to claim 13, wherein said memory access operation includes cache operations.

20. A method according to claim 12, wherein said four operation family bits denote that the function defined in the operation field is user defined.